

SEMICONDUCTOR DEVICE HAVING DUMMY GATES
AND ITS MANUFACTURING METHOD

BACKGROUND OF THE INVENTION

5 Field of the Invention

The present invention relates to a semiconductor device having a plurality of dummy gates and its manufacturing method.

Description of the Related Art

10 Generally, a semiconductor device such as a metal oxide semiconductor (MOS) device is constructed by a gate and source/drain regions manufactured in self-alignment with the gate.

15 In a first prior art method for manufacturing a semiconductor device, a gate conductive layer is deposited on a monocrystalline silicon substrate. Then, a photoresist layer is coated on the gate conductive layer. Then, the photoresist layer is exposed to ultraviolet light via a photomask. In this case, for example, the photomask has a tight pattern such as a comb-shaped gate pattern and a coarse pattern such as an isolated gate pattern. Then, the photoresist layer is developed, so that the photoresist layer is patterned.

20 Next, the gate conductive layer is patterned by an etching process using the photoresist layer as a mask, so that
25 the gate conductive layer is patterned.

Finally, the photoresist layer is removed. Thus, the gate conductive layer has gate patterns corresponding to the gate patterns, respectively. This will be explained later in detail.

30 In the first prior art method, even when the photomask has the same gate length, the gate length of the comb-shaped gate pattern of the gate conductive layer is smaller than the gate length of the isolated gate pattern of the gate conductive layer. This is due to the proximity effect
35 caused by light diffraction and the amount of the gate conductive layer redeposited on the sidewall thereof after the etching process of the gate conductive layer.

In a second prior art method for manufacturing a semiconductor device (see JP-A-10-200109), a dummy gate is interposed between the gates, so as to homogenize the proximity effect and the amount of the redeposited gate
5 conductive layer. This also will be explained later in detail.

In the second prior art method, however, when designing for the dummy gate, an additional design time for dummy patterns thereof is required. In particular, if a plurality of kinds of comb-shaped gate patterns are present,
10 the additional design time is enormously large, which would increase the turnaround time, thus increasing the manufacturing cost.

SUMMARY OF THE INVENTION

15 It is an object of the present invention to provide a semiconductor device having dummy gates and its manufacturing method, capable of reducing the turnaround time.

Another object is to provide a photomask used in
20 such a semiconductor device manufacturing method.

According to the present invention, in a semiconductor device including active areas where transistors are formed and a field area for isolating the active areas from each other, the field area has a plurality of dummy areas where
25 dummy gates are formed.

Also, in a method for manufacturing a semiconductor device, a shallow trench isolation layer is formed in a semiconductor substrate, so that active areas and a field area including dummy areas for isolating the active areas are
30 partitioned. Then, gates are formed on the active areas and dummy gates are formed on the dummy areas.

Further, a photomask is constructed by a gate pattern for forming gates of transistors on a semiconductor substrate, and dummy gate patterns surrounding the gate
35 pattern, for forming dummy gates on the semiconductor substrate. The dummy gate patterns are constructed by a reduction of dummy area patterns for forming a shallow trench

isolation layer in the semiconductor substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be more clearly understood from the description set forth below, as compared with the prior art, with reference to the accompanying drawings, wherein:

Figs. 1A, 1B and 1C are cross-sectional views for explaining a first prior art method for manufacturing a semiconductor device;

Fig. 2 is a plan view illustrating a photomask used in the manufacturing step as illustrated in Fig. 1A;

Figs. 3A, 3B and 3C are cross-sectional views for explaining a first prior art method for manufacturing a semiconductor device;

Fig. 4 is a plan view illustrating a photomask used in the manufacturing step as illustrated in Fig. 3A;

Figs. 5A, 5B and 5C are diagrams for explaining a first step for designing a photomask used in a first embodiment of the method for manufacturing a semiconductor device according to the present invention;

Figs. 6A, 6B and 6C are diagrams for explaining a second step for designing a photomask used in a first embodiment of the method for manufacturing a semiconductor device according to the present invention;

Fig. 7 is a plan view illustrating the semiconductor device obtained by the photomask as illustrated in Figs. 5A, 5B, 5C and Figs. 6A, 6B and 6C;

Figs. 8A through 8K are cross-sectional views for explaining a method for manufacturing the semiconductor device of Fig. 7;

Figs. 9A and 9B are cross-sectional views for explaining the necessity of the dummy gate patterns of Fig. 5C;

Fig. 10 is a plan view illustrating a second embodiment of the semiconductor device according to the present invention; and

Figs. 11A and 11B are plan views for explaining the effect

of the semiconductor device of Fig. 10.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Before the description of the preferred embodiments,
5 prior art semiconductor devices will be explained with
reference to Figs. 1A, 1B, 1C, 2, 3A, 3B, 3C and 4.

Figs. 1A, 1B and 1C are cross-sectional views for
explaining a first prior art method for manufacturing a
semiconductor device using a photomask as illustrated in Fig.
10 2.

First, referring to Fig. 1A, a gate conductive layer
102 made of polycrystalline silicon or the like is deposited
on a monocrystalline silicon substrate 101. Then, a
photoresist layer 103 is coated on the gate conductive layer
15 102. Then, the photoresist layer 103 is exposed to ultraviolet
light via the photomask of Fig. 2. Note that the photomask of
Fig. 2 has a comb-shaped gate pattern GP1 and an isolated gate
pattern GP2. Then, the photoresist layer 103 is developed, so
that the photoresist layer 103 is patterned.

Next, referring to Fig. 1B, the gate conductive
layer 102 is patterned by an etching process using the
photoresist layer 103 as a mask, so that the gate conductive
layer 102 is patterned.

Finally, referring to Fig. 1C, the photoresist
25 layer 103 is removed. Thus, the gate conductive layer 102 has
gate patterns G1 and G2 corresponding to the gate patterns GP1
and GP2, respectively.

In the semiconductor device of Figs. 1A, 1B and 1C
manufactured by the photomask of Fig. 2, even when the
30 photomask of Fig. 2 has the same gate length L, the gate length
L1 of the gate pattern P1 of the gate conductive layer 102 is
smaller than the gate length L2 of the gate pattern P2 of the
gate conductive layer 102. This is due to the following two
reasons. One reason is that the proximity effect caused by
35 light diffraction is larger in the gate pattern P1 than in the
gate pattern P2, since the gate pattern GP1 has closely-
arranged elements while the gate pattern GP2 has a single

element. Another reason is that the amount of the gate conductive layer 102 redeposited on the sidewall thereof after the etching process of the gate conductive layer 102 is larger in the gate pattern P2 than in the gate pattern P1.

5 Figs. 3A, 3B and 3C are cross-sectional views for explaining a second prior art method for manufacturing a semiconductor device using a photomask as illustrated in Fig. 4 (see JP-A-10-200109).

10 First, referring to Fig. 3A, a gate conductive layer 202 made of polycrystalline silicon or the like is deposited on a monocrystalline silicon substrate 201. Then, a photoresist layer 203 is coated on the gate conductive layer 202. Then, the photoresist layer 203 is exposed to ultraviolet light via the photomask of Fig. 4. Note that the photomask of
15 Fig. 4 has dummy gate patterns DP in addition to the comb-shaped gate pattern GP1 and the isolated gate pattern GP2 of Fig. 2. Then, the photoresist layer 203 is developed, so that the photoresist layer 203 is patterned.

20 Next, referring to Fig. 3B, the gate conductive layer 202 is patterned by an etching process using the photoresist layer 203 as a mask, so that the gate conductive layer 202 is patterned.

25 Finally, referring to Fig. 3C, the photoresist layer 203 is removed. Thus, the gate conductive layer 102 has gate patterns G1 and G2 corresponding to the gate patterns GP1 and GP2, respectively, and also, has dummy gates DG corresponding to the dummy gate patterns DP.

30 In the semiconductor device of Figs. 3A, 3B and 3C manufactured by the photomask of Fig. 4, since the photomask of Fig. 4 has the dummy patterns DP, the proximity effect caused by light diffraction is homogenized in the gate pattern P1 and in the gate pattern P2, and also, the amount of the gate conductive layer 202 redeposited on the sidewall thereof after the etching process of the gate conductive layer 202 is
35 homogenized in the gate pattern P2 and in the gate pattern P1. As a result, the gate length L1 of the gate pattern P1 of the gate conductive layer 202 is substantially the same as the gate

length L2 of the gate pattern P2 of the gate conductive layer 202.

In the semiconductor device of Figs. 3A, 3B and 3C manufactured by the photomask of Fig. 4, however, when
5 designing the photomask of Fig. 4, an additional design time for the dummy patterns DP is required. In particular, if a plurality of kinds of comb-shaped gate patterns are present, the additionally designing time is enormously large, which would increase the turnaround time, thus increasing the
10 manufacturing cost.

A first embodiment of the method for manufacturing a semiconductor device will be explained next with reference to Figs. 5A, 5B, 5C, 6A, 6B, 6C and 7.

Figs. 5A, 5B and 5C are diagrams for explaining a
15 method for designing a first photomask M1 used in the first embodiment.

First, referring to Fig. 5A, active area patterns A1 and A2 for forming MOS transistors are set. Note that an area F other than the active area patterns A1 and A2 is defined
20 as a field area pattern for isolating the MOS transistors from each other.

Next, referring to Fig. 5B, square dummy area patterns D arranged in rows and columns are set in the field area F.

Finally, referring to Fig. 5C, the active area patterns A1 and A2 and the dummy area patterns D are combined
25 altogether to complete the first photomask M1.

Figs. 6A, 6B and 6C are diagrams for explaining a
30 method for designing a second photomask M2 used in the first embodiment.

First, referring to Fig. 6A, a comb-shaped gate pattern GP1 and an isolated gate pattern GP2 are set in areas corresponding to the active area patterns A1 and A2,
35 respectively, of Fig. 5A.

Next, referring to Fig. 6B, dummy gate patterns DP are set in areas corresponding to the square dummy patterns D of Fig. 5B. In this case, each of the dummy gate patterns

DP is a reduction of the corresponding square dummy gate area D.

Finally, referring to Fig. 6C, the gate patterns GP1 and GP2 and the dummy gate patterns DP are combined altogether to complete the second photomask M2.

Fig. 7 is a plan view illustrating the semiconductor device obtained by using the photomask M1 of Fig. 5C and the photomask M2 of Fig. 6C.

Note that the dummy gate patterns DP of Fig. 6C are similar to the dummy patterns D of Fig. 5C for forming a shallow trench isolation (STI) layer using a chemical mechanical polishing (CMP) process, which will be explained later. Therefore, if the semiconductor device of Fig. 7 is manufactured by such an STI layer using a CMP process, an additional design for the dummy gate patterns DP requires only a little work, which would not increase the turnaround time.

The method for manufacturing the semiconductor device of Fig. 7 is explained next with reference to Figs. 8A through 8K, which are cross-sectional views taken along the lines X-X and Y-Y in Fig. 7.

First, referring to Fig. 8A, a monocrystalline silicon substrate 1 is thermally oxidized to form a silicon oxide layer 2 thereon. Then, a silicon nitride layer 3 is deposited on the silicon oxide layer 2. Then, a photoresist layer 4 is coated on the silicon nitride layer 3. Then, the photoresist layer 4 is irradiated with ultraviolet light via the photomask M1 of Fig. 5C. Then, the photoresist layer 4 is developed, so that the photoresist layer 4 is patterned.

Next, referring to Fig. 8B, the silicon nitride layer 3 is etched by using the photoresist layer 4 as a mask and the silicon oxide layer 2 as an etching stopper. Then, the silicon oxide layer 2 is etched by using the silicon nitride layer 3 as a mask. Then, the photoresist layer 4 is removed.

Next, referring to Fig. 8C, trenches 5 are perforated in the silicon substrate 1 by etching the silicon substrate 1 using the silicon nitride layer 3 and the silicon oxide layer 2 as a mask.

Next, referring to Fig. 8D, a silicon oxide layer 6 is formed on the entire surface by a thermal oxidation process and a chemical vapor deposition (CVD) process, so that the silicon oxide layer 6 is completely buried in the trenches 5.

Next, referring to Fig. 8E, a CMP process is carried out to flatten the silicon oxide layer 6 using the silicon nitride layer 3 as a stopper.

Next, referring to Fig. 8F, the silicon nitride layer 3 is removed. Then, a CMP process is again carried out to flatten the silicon oxide layer 6, so that the top surface of the silicon oxide layer 6 substantially coincides with the surface of the silicon substrate 1, thus forming STI layers. As a result, areas corresponding to the active area patterns A1 and A2, the field area pattern F and the dummy area patterns D of Fig. 5C are partitioned.

Next, referring to Fig. 8G, after a photoresist pattern layer (not shown) is formed to cover the area A2 and its adjacent area, P-type impurities are implanted into the silicon substrate 1 to form a P-type impurity diffusion region (well) 7 within the silicon substrate 1. Similarly, after a photoresist pattern layer (not shown) is formed to cover the area A1 and its adjacent area, N-type impurities are implanted into the silicon substrate 1 to form an N-type impurity diffusion region (well) 8 within the silicon substrate 1. In this case, note that the impurity type of the dummy areas D can be of a P-type or an N-type.

Next, referring to Fig. 8H, a gate conductive layer 9 made of polycrystalline silicon or the like is deposited by a CVD process or a sputtering process. Then, an anti-reflection coating (ARC) layer 10 made of organic material is coated on the gate conductive layer 9. Then, a photoresist pattern layer 11 is coated on the ARC layer 10, and is irradiated with ultraviolet light via the photomask M2 of Fig. 6C. Then, the photoresist layer 11 is developed and patterned as illustrated in Fig. 8H. In this case, due to the dummy patterns DP, the length L1 of the photoresist layer 11(GP1)

of the active area A1 and the length L2 of the photoresist layer 11(GP2) of the active area A2 are homogenized regardless of the proximity effect.

5 Next, referring to Fig. 8I, the ARC layer 10 and the gate conductive layer 9 are sequentially etched by using the photoresist layer 11 as a mask.

Next, referring to Fig. 8J, the photoresist layer 11 and the ARC layer 10 are sequentially removed.

10 Finally, referring to Fig. 8K, after a photoresist pattern layer (not shown) is formed to cover the N-type diffusion region 8, N-type impurities are implanted into the silicon substrate 1 in self-alignment with the gate conductive layer 9(GP1), to form N⁺-type regions 11 within the P-type impurity region 7. Similarly, after a photoresist pattern layer (not shown) is formed to cover the P-type diffusion region 7, P-type impurities are implanted into the silicon substrate 1 in self-alignment with the gate conductive layer 9(GP2), to form P⁺-type regions 12 within the N-type impurity region 7. Then, a boron-included phosphor-silicate glass (BPSG) layer 13 is deposited on the entire surface by a CVD process, and contact holes CONT are perforated in the BPSG layer 13. Then, connection layers 14 are formed and connected via the contact holes CONT to the corresponding impurity diffusion regions.

25 The necessity of the dummy area patterns D of the photomask M1 of Fig. 5C is explained with reference to Figs. 9A and 9B.

30 If the dummy area patterns D are absent in the photomask M1 of Fig. 5C, as illustrated in Fig. 9A, which corresponds to Fig. 8D, a trench 5' is formed in the entire field area F. Therefore, after the silicon oxide layer 2, the silicon nitride layer 3 and the silicon oxide layer 6 are formed, a CMP process is carried out so that an STI layer 6(STI) is buried in the trench 5' as illustrated in Fig. 9B. However, 35 in this case, the STI layer 6(STI) becomes indented. This deteriorates the reliability of wiring (connection) layers formed on the STI layer 6(STI). Thus, the dummy area patterns

D are indispensable for manufacturing an STI-structured semiconductor device using a CMP process.

In Fig. 10, which illustrates a second embodiment of the present invention, the rows of the dummy area patterns D and the dummy gate patterns DP along the X-direction are shifted from each other. As a result, the parasitic capacitance of wiring (connection) layers L1 and L2 formed over the dummy gate patterns DP is homogenized, which would improve the characteristics. That is, as illustrated in Fig. 11A which schematically shows the wiring layers L1 and L2 in a case of the first embodiment, the parasitic capacitance of the wiring layer L1 is larger than the parasitic capacitance of the wiring layer L2. On the other hand, as illustrated in Fig. 11B which schematically shows the wiring layers L1 and L2 in a case of the second embodiment, the parasitic capacitance of the wiring layer L1 is substantially the same as that of the wiring layer L2.

In the above-described second embodiment, the columns of the dummy area patterns D and the dummy gate patterns DP along the Y-direction can be shifted from each other. Also, the rows and columns of the dummy area patterns D and the dummy gate patterns DP along the X-direction and the Y-direction can be both shifted from each other. Further, the dummy area patterns D and the dummy gate patterns DP can be sloped.

Additionally, the dummy area patterns D and the dummy gate patterns DP can be rectangular, polygonal or circular.

As explained hereinabove, according to the present invention, since dummy gate patterns are derived from dummy area patterns so that an additional design time for the dummy gate patterns is reduced, the turnaround time can be decreased, thus decreasing the manufacturing cost.